REMARKS

This application has been carefully reviewed in light of the Office Action dated February 12, 2004. Claims 1-15 and 17-18 remain in this application. Claim 1 is the independent Claim. Claims 1, 13 and 15 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Interview Summary

Applicants thank the Examiner for the courtesies extended during the telephone interview of April 1, 2004. Applicants have amended the claims as discussed during the telephone interview and, as also discussed during the telephone interview, submit that those claims are now in condition for allowance.

Claim Objection

Claim 15 was objected to because of an informality. In response, Applicants have amended that claim to addresses the concern of above objection. Reconsideration and withdrawal of the above objection are respectfully requested.

Non-Art Based Rejections

Claims 13 and 14 were rejected under 35 U.S.C. § 112, second paragraph for indefiniteness. In response, Applicants have amended those claims in accordance with the Examiner's suggestions. Reconsideration and withdrawal of the above § 112 rejections are respectfully requested.

Art-Based Rejections

Claims 1-6 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6,479,905 (Song); Claims 17-18 were rejected under 35 U.S.C. § 103(a) over Song; Claims 1-6, 8-10, 17 and 18 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,507,079 (Komori). Applicants respectfully traverse the rejections and submit that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Song Reference

Song is directed to a full CMOS SRAM cell which includes first and second active regions formed in a semiconductor substrate. (*See, Song, abstract; Col. 1, lines 2-5*). Song discloses a semiconductor device in which the first drain-gate wiring layer 9i' and the second drain-gate wiring layer 9i" are located on the same layer level. (*See, Song, Figure 5; Col. 5, lines 26-31*).

The Komori Reference

Komori is directed to a static semiconductor memory device and an SRAM capable of preventing soft errors (*See, Komori, abstract; Col. 1, lines 7-11*). Komori discloses a semiconductor device in which the first drain-gate wiring layer 111 and the second drain-gate wiring layer 116 are located on the same layer level. (*See, Song, Figure 40; Col. 2, lines 7-41*).

The Claims are Patentable Over the Cited References

The present application is generally directed to semiconductor devices such as static random access memories (SRAMs).

As defined by amended independent Claim 1, a semiconductor device is provided with a memory cell including a first driver transistor, a second driver

transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor. The semiconductor device includes a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor. A second gate-gate electrode layer includes a gate electrode of the second load transistor and a gate electrode of the second driver transistor. A first drain-drain wiring layer forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor. A second drain-drain wiring layer forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor. A first drain-gate wiring layer forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer. A second drain-gate wiring layer forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer. A first active region provides the first load transistor. The first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively. A first protruded active region is provided in a manner to protrude from an end portion of the first active region.

The applied art of the record are not seen to disclose the above features of the present invention. In particular, the applied art of the record are not seen to disclose or suggest "wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively," as required by the claims of the present invention.

Song, cited by the Office Action is directed to a full CMOS SRAM cell which includes first and second active regions formed in a semiconductor substrate. (*See, Song, abstract; Col. 1, lines 2-5*). Song discloses a semiconductor device in which the first drain-gate wiring layer 9i' and the second drain-gate wiring layer 9i" are

located on the same layer level. (*See, Song, Figure 5; Col. 5, lines 26-31*). Song does not, however, disclose or even suggest "wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively," as required by the claims of the present invention.

Komori, also cited by the Office Action, is directed to a static semiconductor memory device and an SRAM capable of preventing soft errors (*See, Komori, abstract; Col. 1, lines 7-11*). Komori discloses a semiconductor device in which the first drain-gate wiring layer 111 and the second drain-gate wiring layer 116 are located on the same layer level. (*See, Song, Figure 40; Col. 2, lines 7-41*). However, Komori does not disclose or even suggest "wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively," as required by the claims of the present invention.

Since the cited reference fails to disclose, teach or suggest the above features recited in amended independent Claim 1, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, amended independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

The remaining claims depend either directly or indirectly from amended independent Claim 1 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

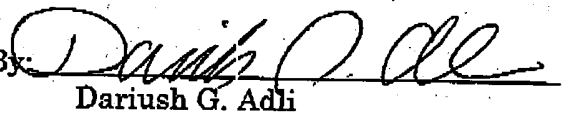
If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: May 11, 2004

By: 

Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701